

FIG.1

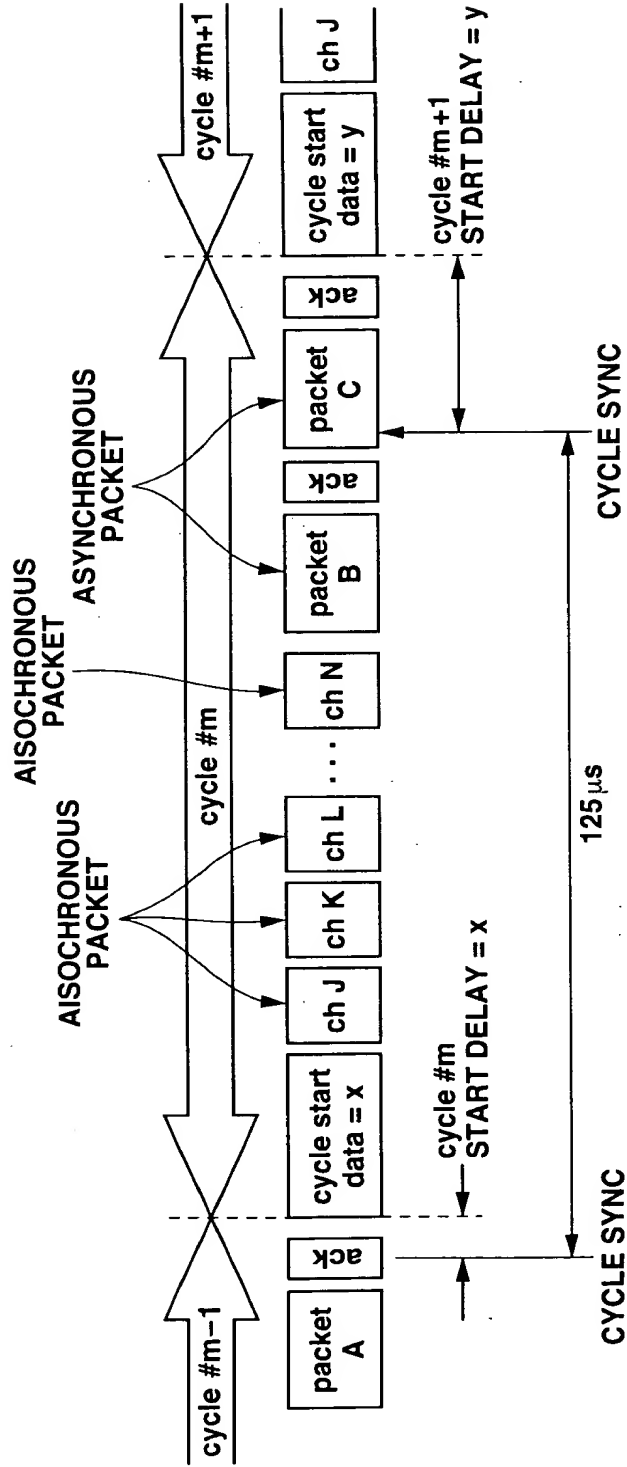


FIG.2

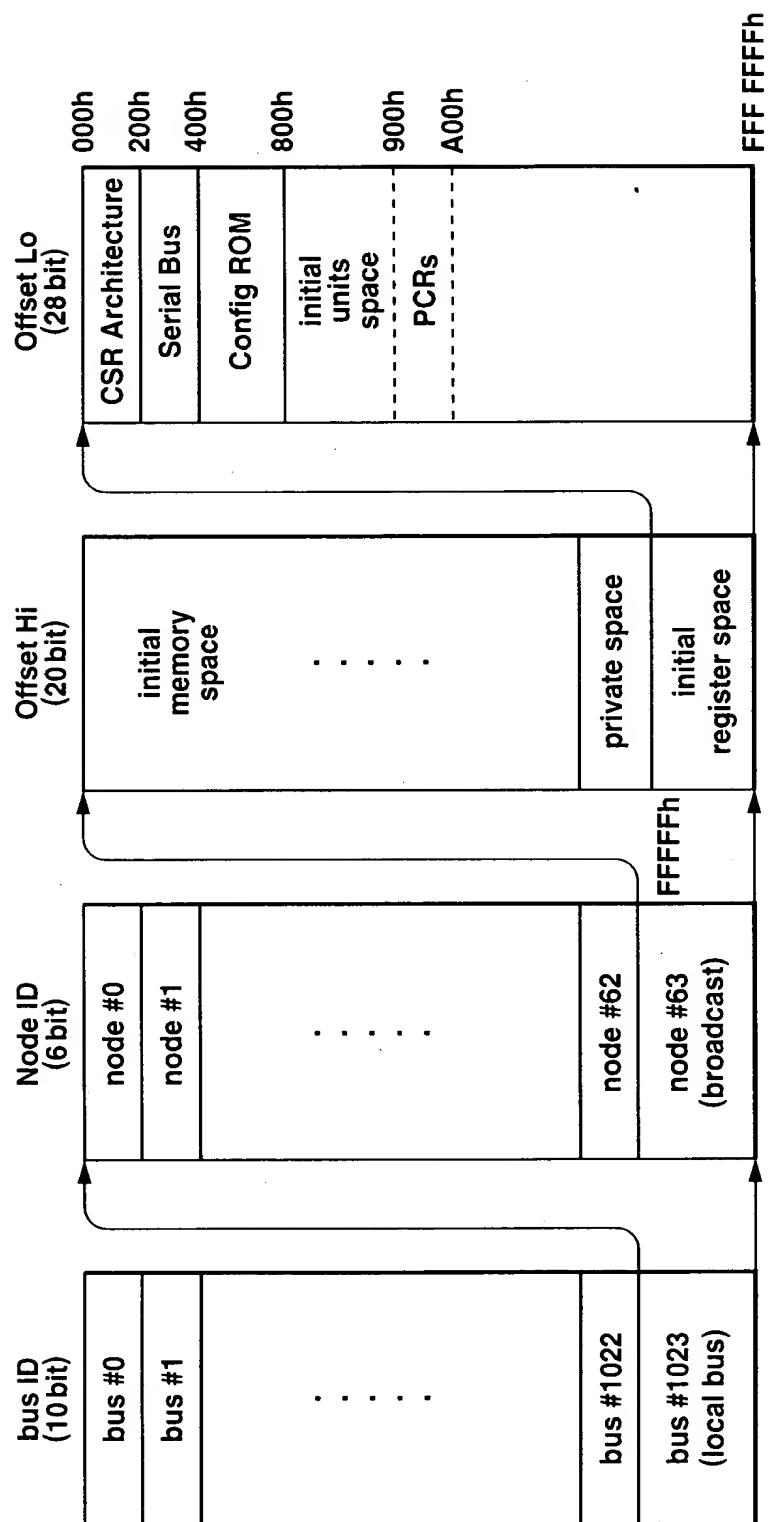


FIG.3

OFFSET	NAME	OPERATION
000h	STATE_CLEAR	STATUS AND CONTROL INFORMATION
004h	STATE_SET	SET STATE_CLEAR BIT
008h	NODE_IDS	INDICATES 16-BIT NODE ID
00Ch	RESET_START	STARTS COMMAND RESET
018h-01Ch	SPLIT_TIMEOUT	PROVIDES MAX SPLIT TIME
200h	CYCLE_TIME	CYCLE TIME
210h	BUSY_TIMEOUT	PROVIDES RETRY LIMITATION
21Ch	BUS_MANAGER	INDICATES BUS MANAGER ID
220h	BANDWIDTH_AVAILABLE	INDICATES BAND ALLOCATABLE TO AISOCHRONOUS COMMUNICATION
224h-228h	CHANNELS_AVAILABLE	INDICATES USING STATE OF EACH CHANNEL

FIG.4

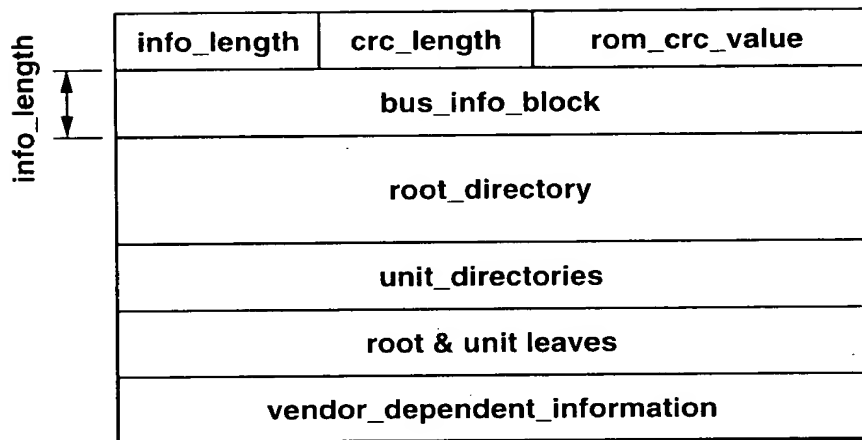


FIG.5

400h	04h	crc_length	rom_crc_value
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Bus_info_block

404h	"1394"							
408h	lmc	cmc	isc	bmc	reserved	cyc_clk_acc	max_rec	reserved
40Ch	Company_ID							Chip_ID_hi
410h	Chip_ID_lo							

Root_directory

414h	root_length		CRC	
418h	03h	module_vendor_id		
41Ch	0Ch	node_capabilities		
420h	8Dh	node_unique_id offset		
424h	D1h	unit_directory offset		
428h	Optional.			
:				
:				

Unit_directory

unit_directory_length		CRC	
12h	unit_spec_id		
13h	unit_sw_version		
		Optional.	

FIG.6

900h	Output Master Plug Register
904h	Output Plug Control Register #0
908h	Output Plug Control Register #1
⋮	⋮
97Ch	Output Plug Control Register #30
980h	Input Master Plug Register
984h	Input Plug Control Register #0
988h	Input Plug Control Register #1
⋮	⋮
9FCh	Input Plug Control Register #30

FIG.7

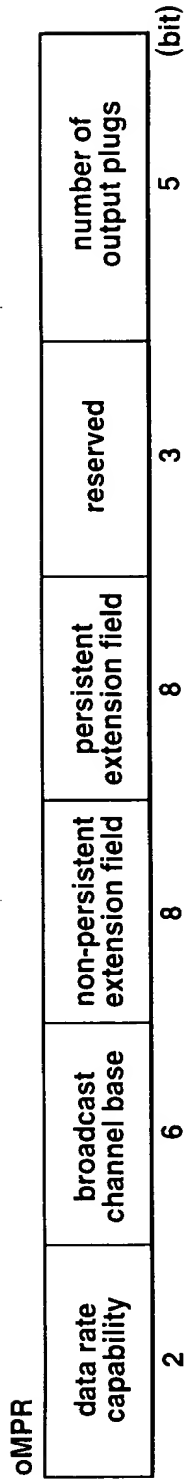


FIG. 8A

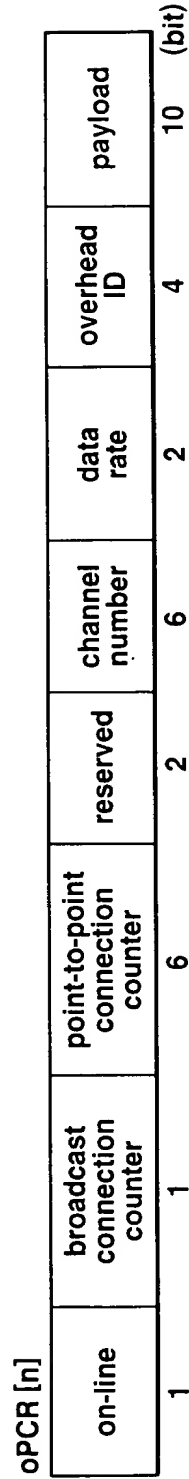


FIG. 8B

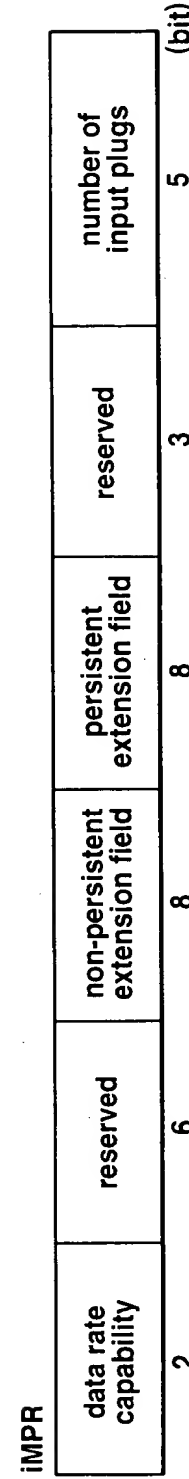


FIG. 8C

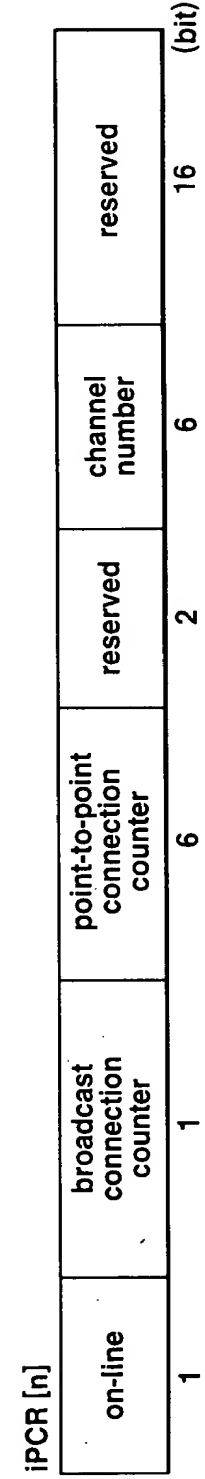


FIG. 8D

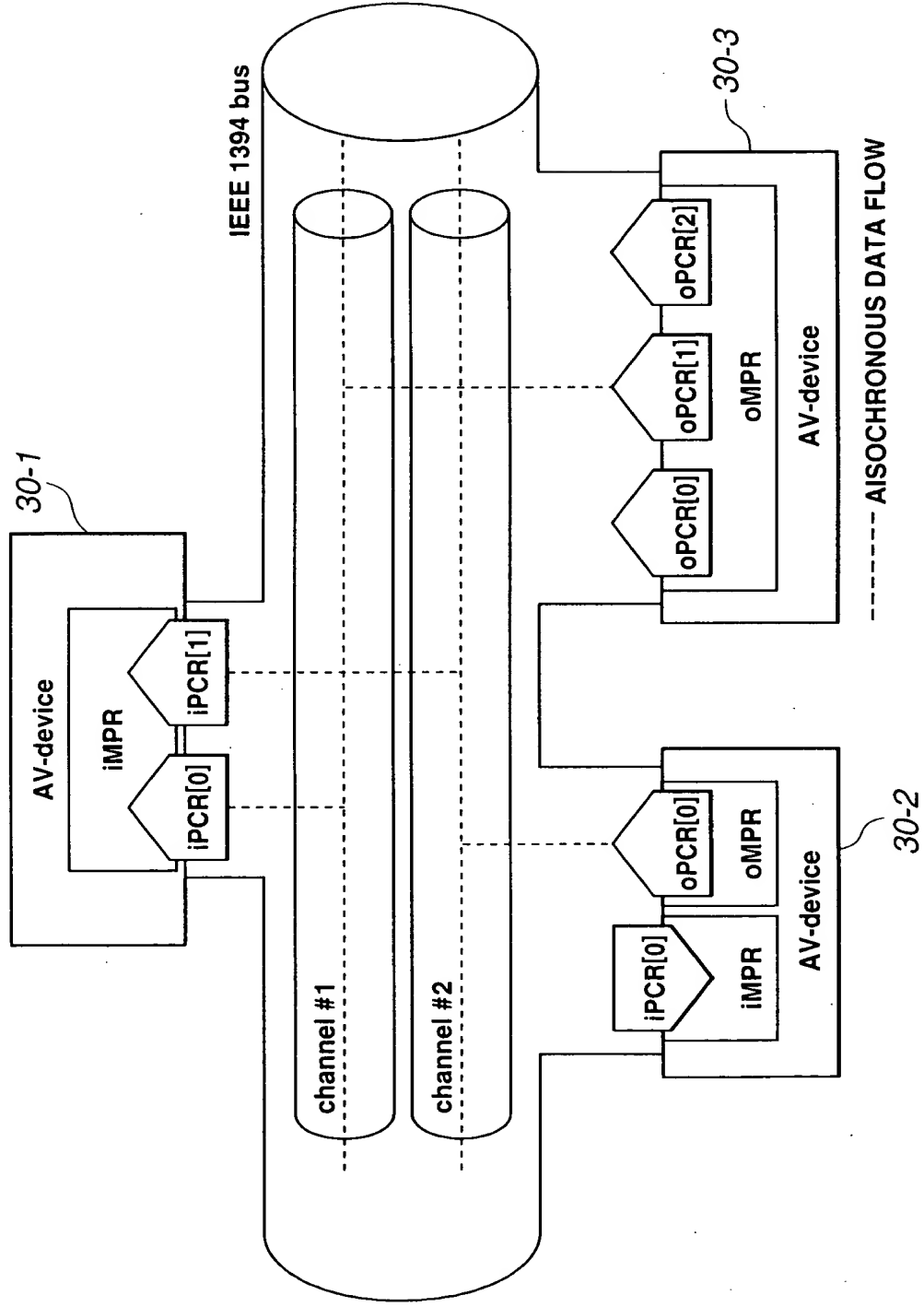


FIG.9

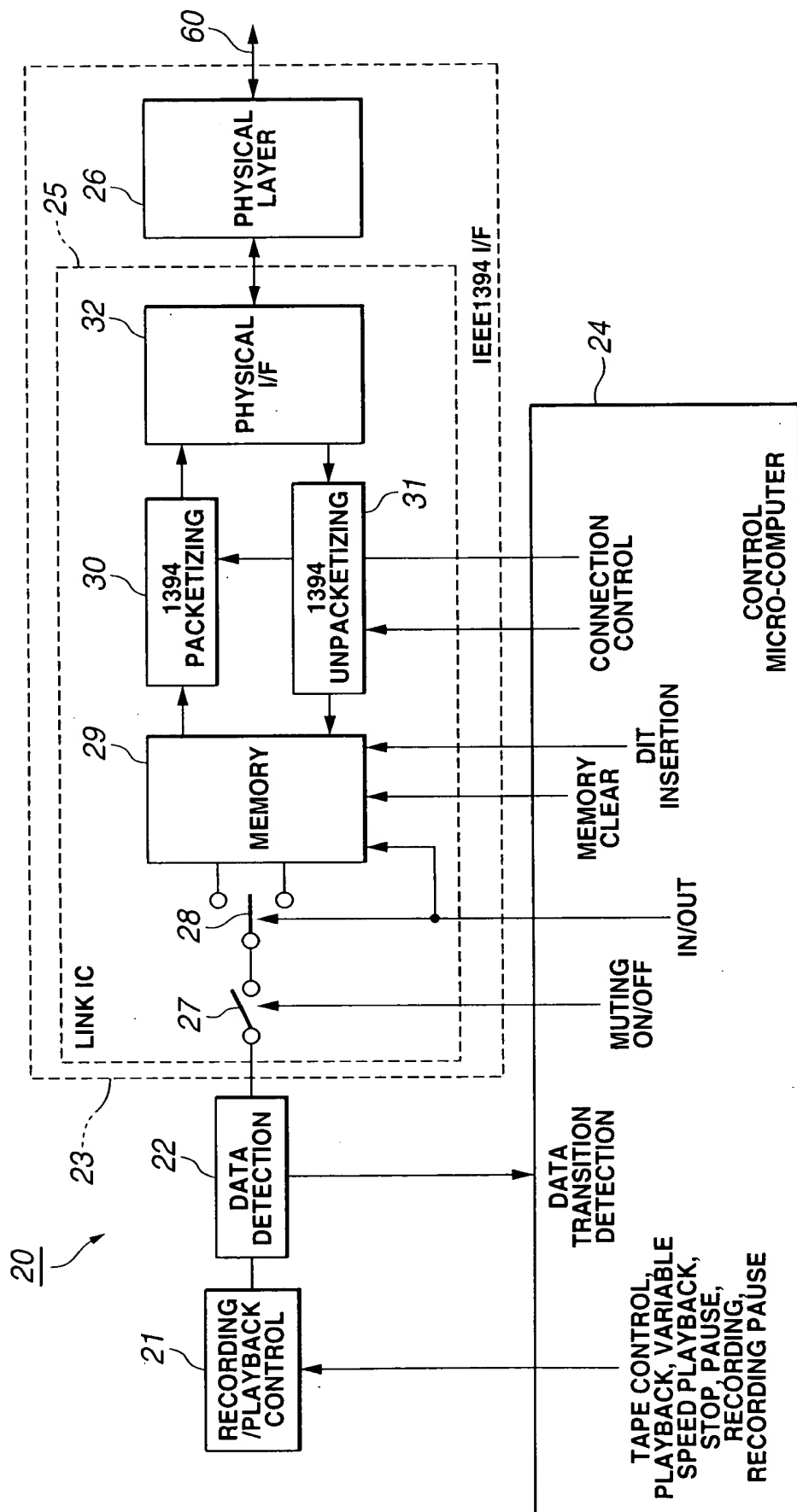


FIG.10

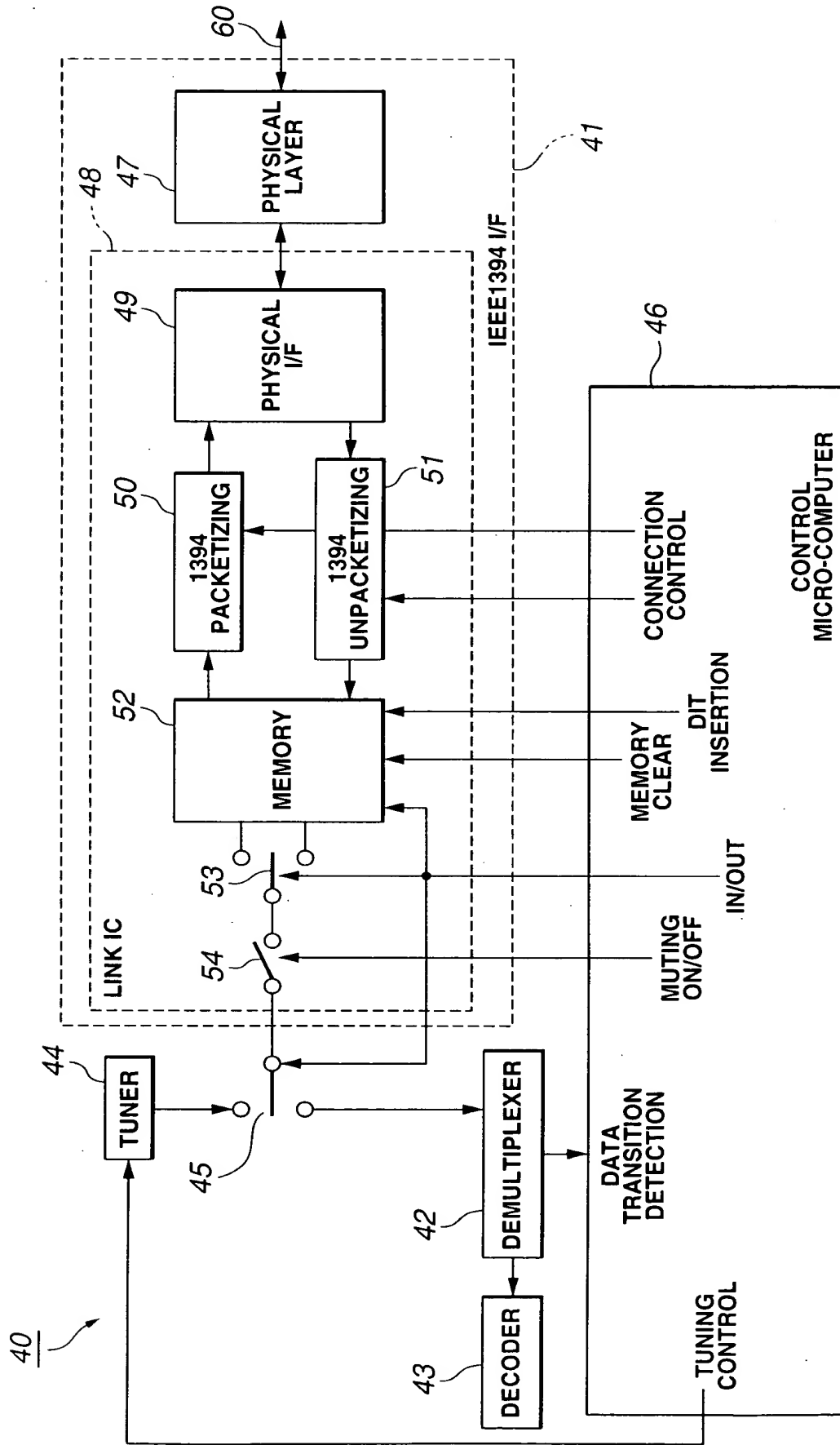


FIG.11

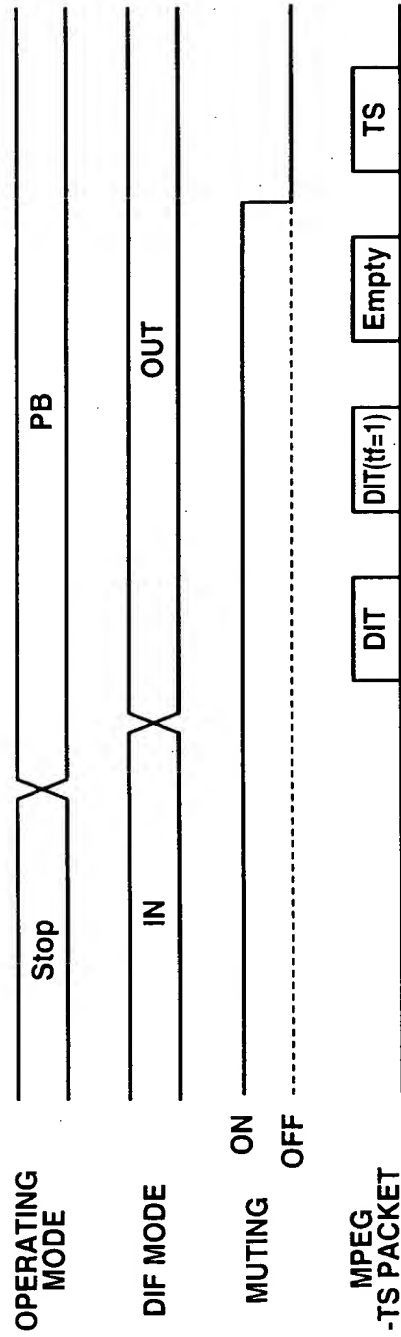


FIG.12

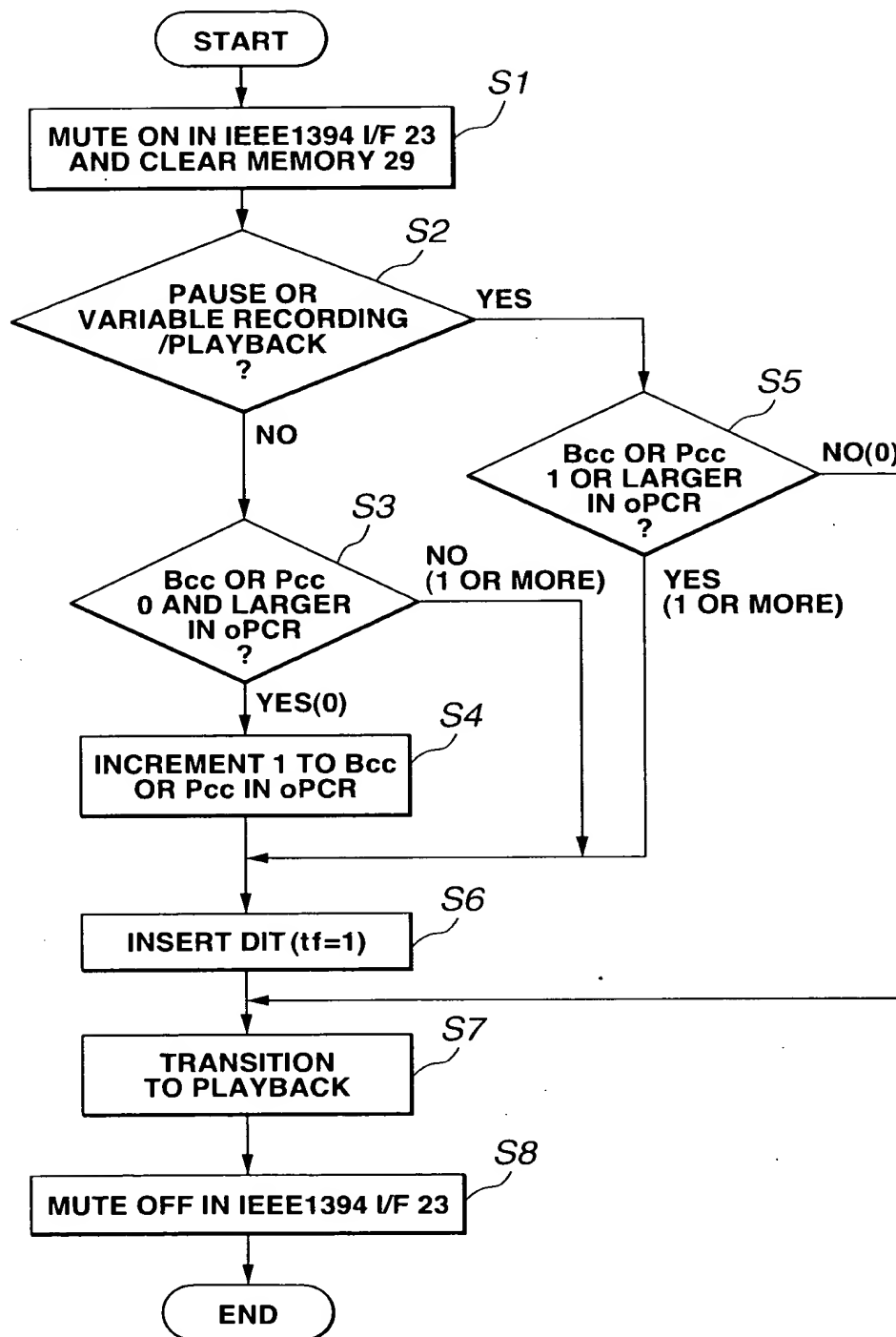


FIG.13

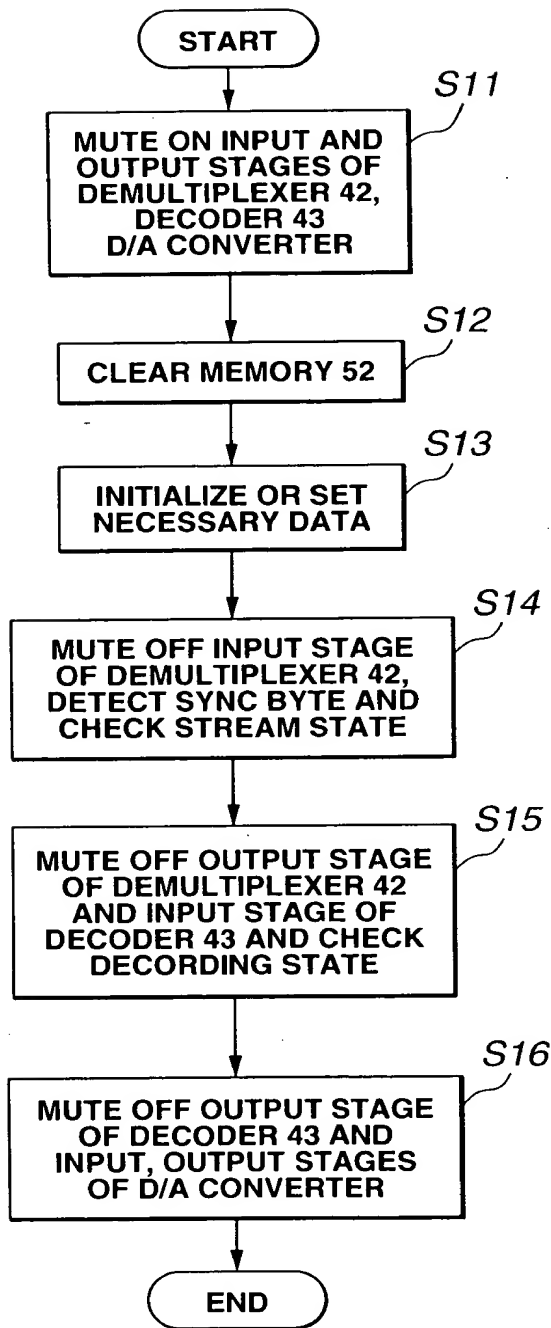


FIG.14

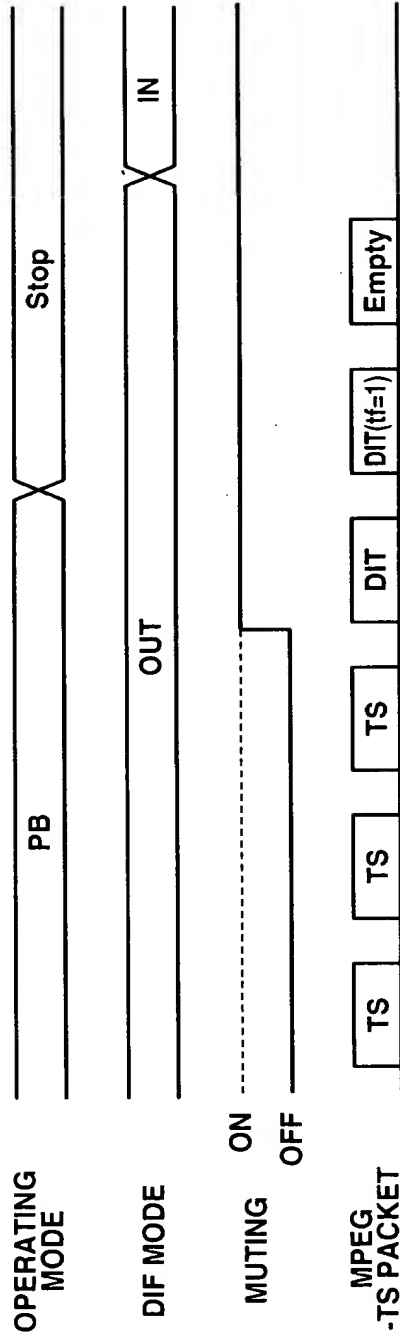


FIG.15

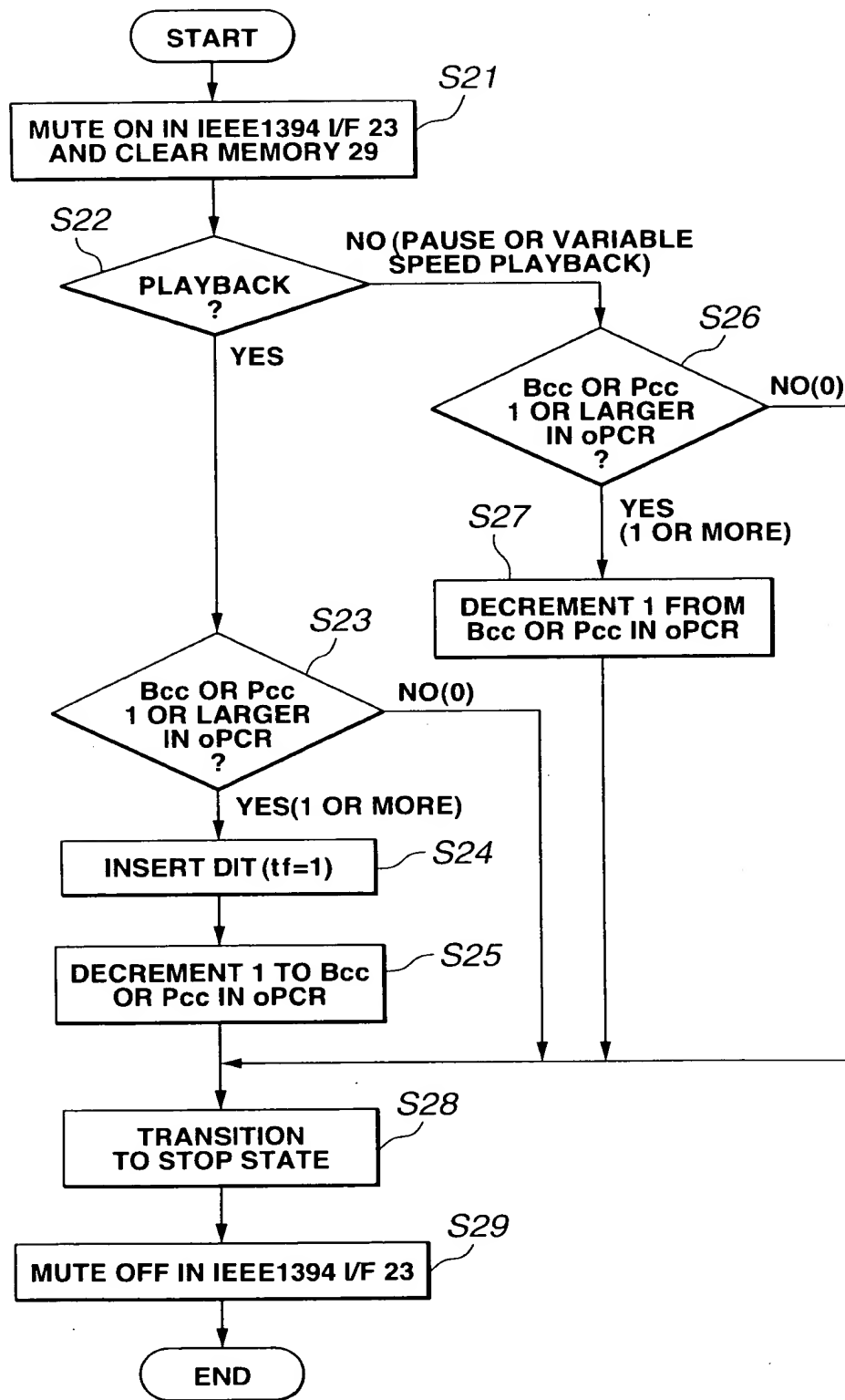


FIG.16

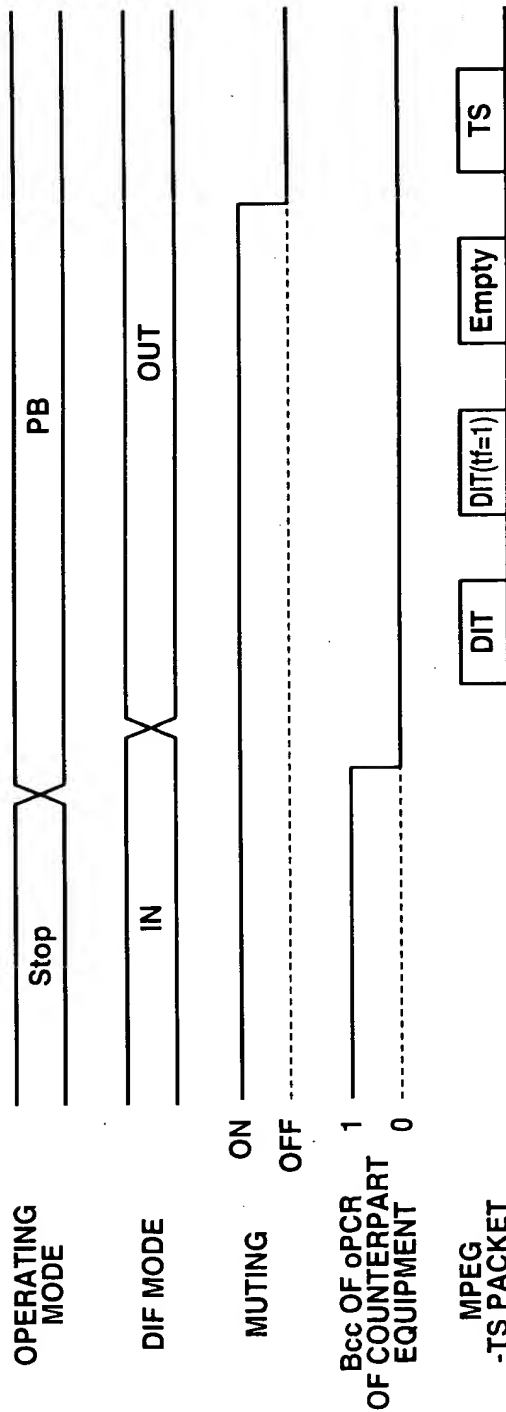


FIG.17

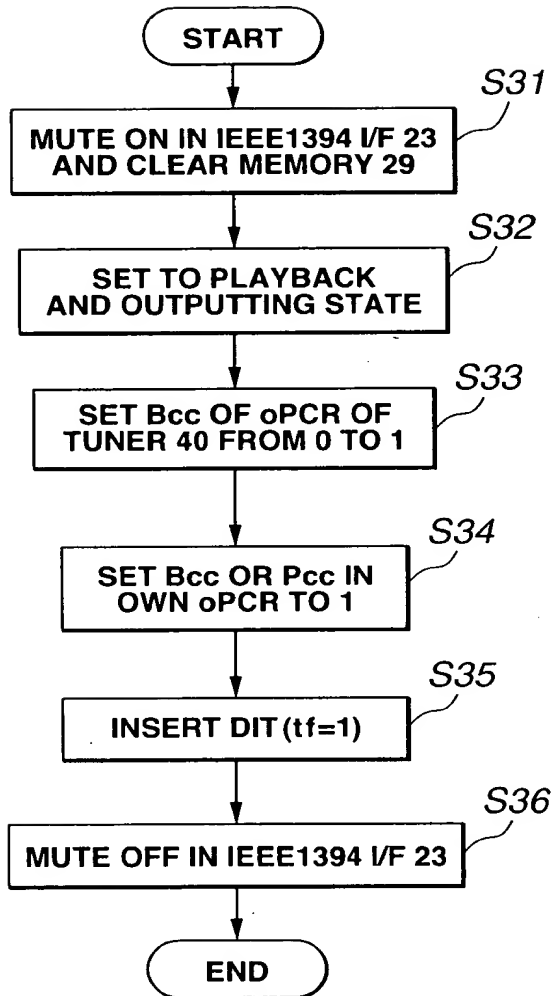


FIG.18

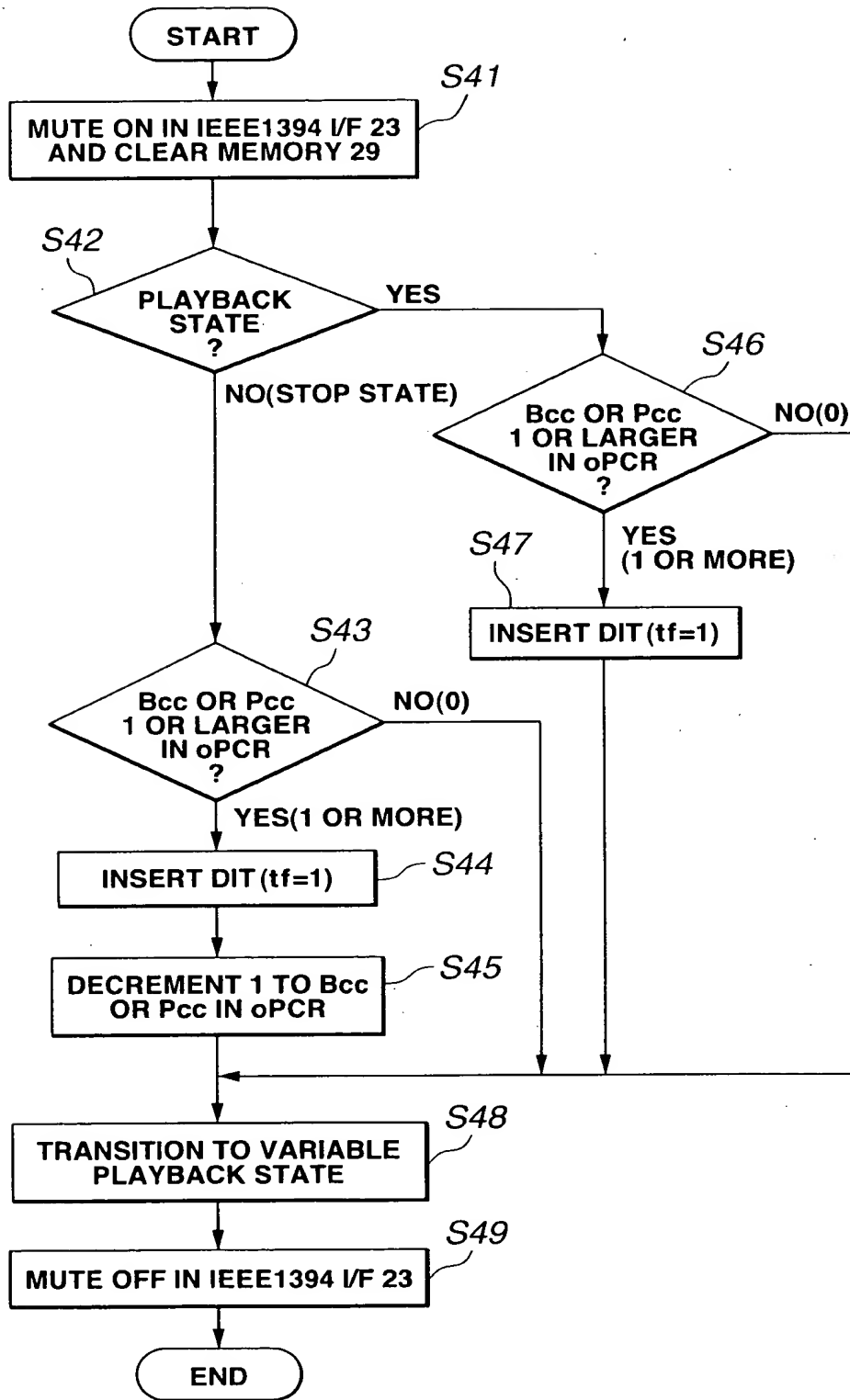


FIG.19

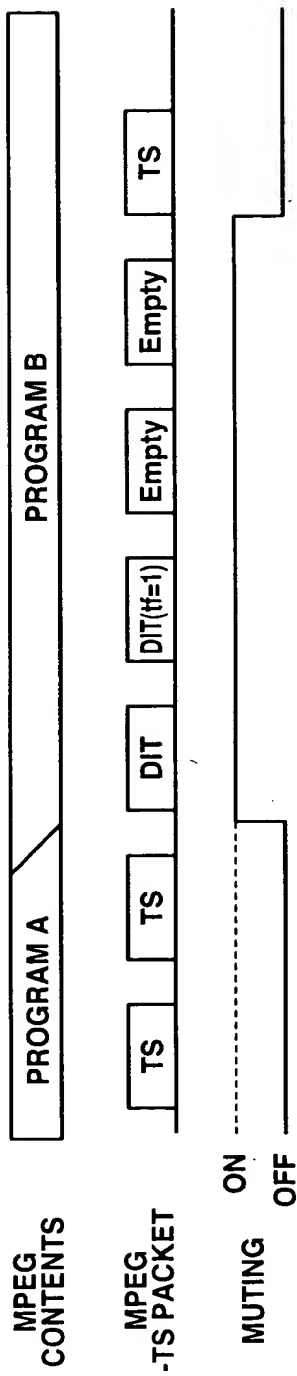


FIG.20

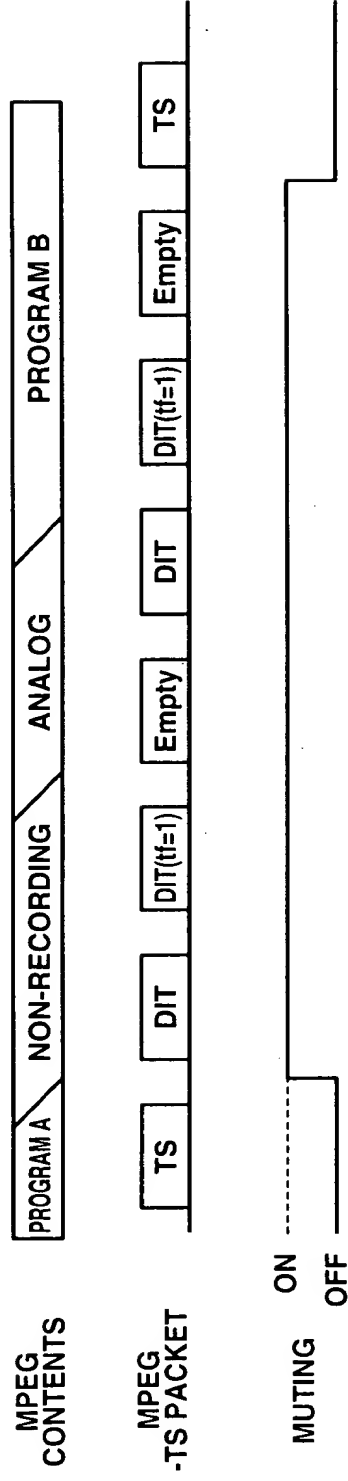


FIG.21

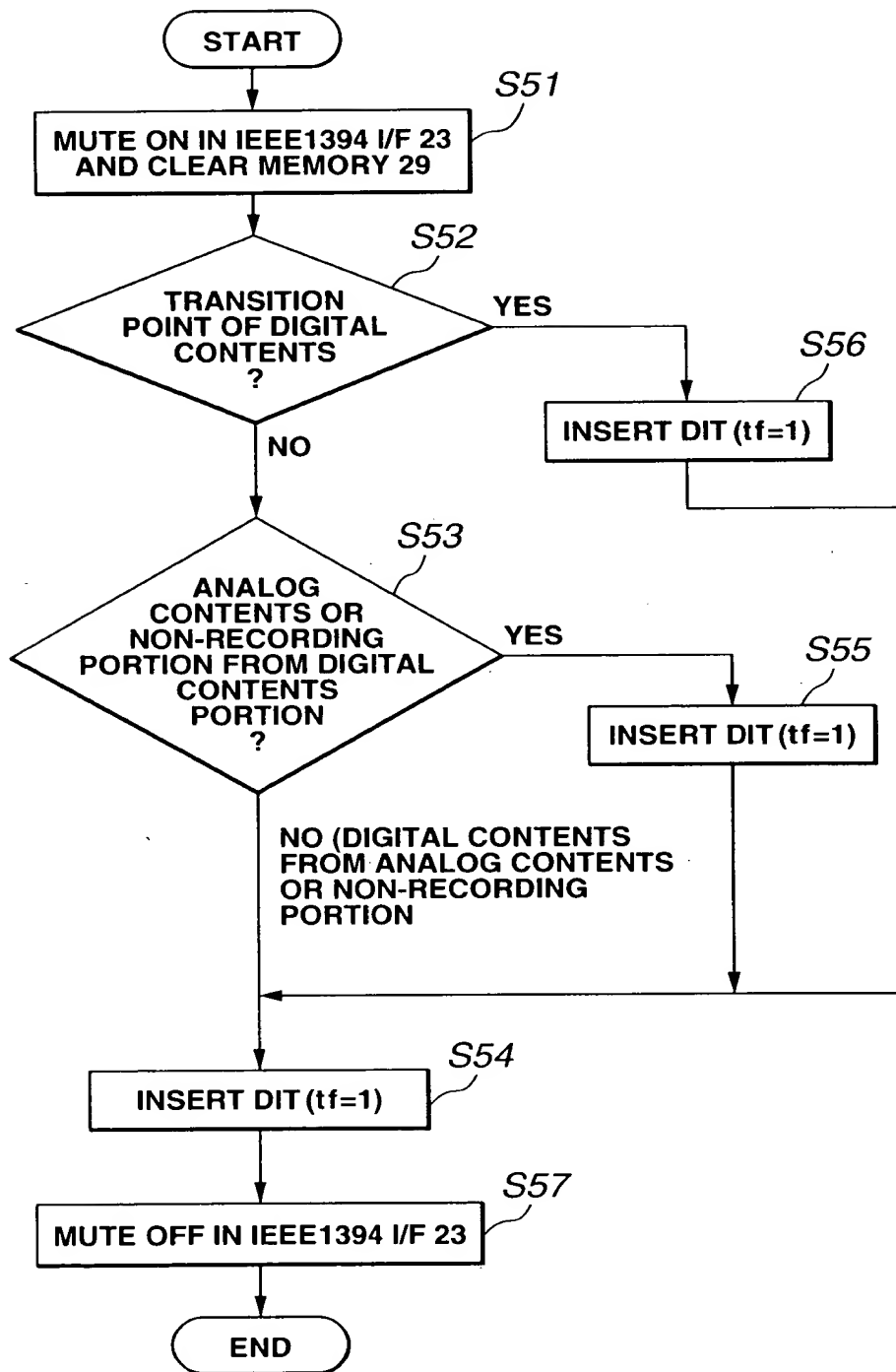


FIG.22